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LOW POWER CONTROL CIRCUIT AND METHOD FOR A MEMORY DEVICE

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LOW POWER CONTROL CIRCUIT AND METHOD FOR A MEMORY DEVICE

FIELD OF THE INVENTION

[0001] The invention relates generally to semiconductor memory devices, and more particularly to an improved method and apparatus for allowing grounded Vref voltages during low power modes of a semiconductor memory device.

BACKGROUND

[0002] There is a demand for faster, higher capacity, random access memory (RAM) devices. RAM devices, such as dynamic random access memory (DRAM) devices are typically used as the main memory in computer systems. Although the operating speed of the DRAM has improved over the years, the speed has not reached that of the processors used to access the DRAM.

[0003] Synchronous dynamic random access memory (SDRAM) has been developed to provide faster operation in a synchronous manner. SDRAMs are designed to operate synchronously with the system clock. That is, input and output data of the SDRAM are synchronized to an active edge of the system clock which is driving the processor accessing the SDRAM.

[0004] Double data rate (DDR) SDRAMs and second generation DDR SDRAMs, known as DDR II SDRAMs, are being developed to provide twice

the operating speed of the conventional SDRAM. These devices allow data transfers on both the rising and falling edges of the system clock and thus, provide twice as much data as the conventional SDRAM.

[0005] It is desirable that DDR SDRAM devices are operated in accordance with industry standards, such as the Stub Series Terminated Logic for 2.5V (SSTL_2) standard. By adhering to industry standards, the DDR SDRAM devices are assured of being compatible with other industry components that also adhere to the standards. This way, components from different manufacturers may be integrated into the same system without adversely impacting the performance of the system.

[0006] Current standards dictate that DDR SDRAM devices have "low" power operations such as e.g., power-down and self-refresh operations. These low power operations are initiated when a clock enable control signal (CKE), which activates and deactivates an internal clock of the DDR SDRAM, is received having a value that disables the internal clock. During a power-down condition, the specification indicates that all input buffers should be disabled with the exception of input buffers used for the clock enable CKE and differential clock input signals CK, CK#. During self-refresh, the specification indicates that all input buffers should be disabled with the exception of input buffers used for the clock enable signal CKE. The enabled input buffers, however, draw current, which is undesirable.

[0007] Moreover, DDR SDRAM devices use a specified reference voltage (Vref) in its input receiver and buffers. The reference voltage Vref is usually connected to a first input of a differential amplifier while a second

input of the amplifier is connected to command, address or data lines. The reference voltage Vref is used to determine whether the received command, address or data has a value of logic 0 or logic 1. The amplifier, however, draws current. It is desirable to reduce the current being drawn in the low power operating modes.

[0008] Furthermore, it is desirable to ground or float the reference voltage Vref in the low power operating mode to reduce the overall power consumption of the system that the DDR SDRAM device is used in during the low power modes. Grounding or floating the reference voltage Vref, however, adversely affects the operation of the DDR SDRAM's differential amplifiers, used in the remaining activated buffers, since a small input signal, noise or other glitch can cause the differential amplifier to output a logic 1 instead of a logic 0. For example, if noise were present on the differential amplifier input connected to receive the clock enable signal CKE, the amplifier will output a logic 1 instead of 0, which takes the SDRAM out of the low power mode because the device thinks that a clock enable signal CKE with a value enabling the internal clock has been received. Moreover, the device is susceptible to being repetitively placed into and taken out of the low power mode if there is noise or some other glitch in the device. These scenarios are undesirable and are contrary to the industry standards.

[0009] Another technique uses additional TTL logic, such as a TTL buffer or inverter to detect when the clock enable signal CKE is received during low power modes. The TTL buffer does not rely on a comparison to the reference voltage Vref, but has other problems. For example, the clock

enable signal CKE is specified by the industry standard as a differential signal, but the buffer is not a differential buffer. If noise were present on the line carrying the clock enable signal CKE to the TTL buffer, the buffer trip point could be reached causing the buffer to output a logic 1 instead of 0, which takes the SDRAM out of a low power mode. This is undesirable and is contrary to the industry standards.

[0010] Accordingly, there is a need and desire for an improved method and apparatus that reduces power when operating a DDR SDRAM in a low power operating mode such as power-down or self-refresh.

SUMMARY

[0011] The present invention provides a method and apparatus that reduces power in a memory device when operating the device in a low power operating mode.

[0012] The above and other features and advantages are achieved in various embodiments of the invention by providing a memory device with a low power control circuit that reduces power in the device while ensuring that the device remains in a low power mode until a high power mode has been requested. The low power control circuit initially monitors a control signal using a CMOS buffer or inverter while a reference voltage is grounded or floated. Upon CMOS buffer detection of a signal indicating that a high power mode is required, the low power control circuit monitors the signal using a differential amplifier and the specified reference voltage (i.e., ungrounded and un-floated reference voltage) to determine if the low power

mode should be exited. In doing so, the low power control circuit prevents noise from inadvertently causing the device to exit the low power mode while at the same time reduces the power in the device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The foregoing and other advantages and features of the invention will become more apparent from the detailed description of exemplary embodiments provided below with reference to the accompanying drawings, in which:

[0014] FIG. 1 is a block diagram illustrating a double data rate (DDR) synchronous dynamic random access memory (SDRAM) device constructed in accordance an exemplary embodiment of the invention;

[0015] FIG. 2 is a block diagram of a lower power control circuit, used in the FIG. 1 device, constructed in accordance with an exemplary embodiment of the invention;

[0016] FIG. 3 is a block diagram of a lower power control circuit, used in the FIG. 1 device, constructed in accordance with another exemplary embodiment of the invention;

[0017] FIG. 4 shows a processor system incorporating at least one DDR SDRAM constructed in accordance with an embodiment of the invention; and

[0018] FIG. 5 is an exemplary timing diagram for an exemplary embodiment of the invention.

DETAILED DESCRIPTION

[0019] In the following detailed description, reference is made to the accompanying drawings, which are a part of the specification, and in which is shown by way of illustration various embodiments whereby the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention. It is to be understood that other embodiments may be utilized, and that structural, logical, and electrical changes, as well as changes in the materials used, may be made without departing from the spirit and scope of the present invention.

[0020] Now referring to the figures, where like reference numbers designate like elements, FIG. 1 shows a DDR SDRAM 100 constructed in accordance with an exemplary embodiment of the invention. The SDRAM 100 includes control logic 10, address registers 20, a row-address multiplexer 22, refresh counter 32, row decoders 24, bank control logic 26, column address counters/latch 28, column decoders 30, I/O (input/output) gating and mask logic 40, sense amplifier circuits 44, memory banks 50, and input/output circuitry 60. In the illustrated embodiment, four memory banks 50, sense amplifier circuits 44, column decoders 30 and row decoders 24 are used in the SDRAM 100. It should be appreciated that the invention can utilize one, two, four, eight or more memory banks 50 and associated amplifiers and decoders.

[0021] The address registers 20 input a bank address BA0, BA1 and an address A0-A10. Depending upon the command, the address A0-A10 is either a row address or column address. The address registers 20 output a

row address RA, column address CA and bank address BA. The bank address BA is sent to the bank control logic 26, which sends an activation signal to the row and column decoder 24, 30 associated with the bank address BA. The row address RA is sent to the row-address multiplexer 22, which sends the address RA to the activated row decoder 24. As is known in the art, the row decoder 24 will activate the appropriate row of memory in its associated bank 50. The column address CA is sent to the column address counter/latch 28, which sends the address CA to the activated column decoder 30. The latch 28 also outputs the least significant bit CA0 of the column address CA. As is known in the art, the column decoder 30 will activate the addressed column of the appropriate bank of memory 50 (through the I/O gating and mask logic 40 and the sense amplifiers 44). This addressing scheme is used for read and write operations.

[0022] The input/output circuitry 60 is connected to the I/O gating and mask logic 40. The input/output circuitry 60includes a read latch 62, write FIFO and drivers 64, multiplexer 66, DQS generator 68, input registers 70, a delayed lock loop (DLL) 72, drivers 74 and receivers 76. The drivers 74 receive data DATA read from addressed memory location from one of the banks 50 through the logic 40, latch 62 and multiplexer 66. CA0 is used to control the multiplexer 66. The drivers 74 also receive a data strobe DQS strobe from the DQS generators 68. The drivers 74 output the DATA and data strobe DQS to an external device through input/output pins DQ0-DQ31 and the DQS pin.

[0023] Data to be written into the SDRAM 100 is input to the receivers 76 through input/output pins DQ0-DQ31 when the data strobe DQS is received. Masking information DM0-DM3 may also be received. The received data or masking information DM0-DM3 is sent to the write FIFO and drivers 64 via the input registers 70 (controlled by CA0) and eventually written into the addressed location in one of the banks 50 (addressing described above).

[0024] The control logic 10 includes mode registers 12, a conventional command decoder 14 and a lower power control circuit 200. The registers 12 and command decoder 14 are used to interpret input control signals and drive the remaining circuitry of the SDRAM 100. The low power control circuit 200 is used to reduce power in the SDRAM 100 while ensuring that the SDRAM 100 remains in a low power mode until a high power mode has been requested. The construction and operation of low power control circuit 200 is discussed below in more detail with respect to FIG. 2.

[0025] As is known in the art, the control logic 10 inputs the clock enable signal CKE as well as differential clock signals CK, CK#, chip select CS#, write enable WE#, column address strobe CAS# and row address strobe RAS# signals (the # designation indicates that the signal is active low). The CAS#, RAS#, WE#, and CS# signals define the commands received by the control logic 10 while the CK, CK# and CKE signals are used to synchronize the operation of the SDRAM 100 to the external system clock.

[0026] Distinct combinations of the control signals constitute distinct commands. For example, the combination of RAS# low, CAS# high and WE#

low represents a precharge command. Examples of other well known commands include, but are not limited to, the active, read, write, burst terminate, auto refresh (or self refresh), load mode register, and NOP commands.

[0027] As noted earlier, the clock enable signal CKE is used to place the SDRAM 100 into a lower power mode for self-refresh or power down operations. Self refresh is initiated when the auto refresh command is received and the clock enable signal CKE is low. If the clock enable signal CKE is not low, then an auto refresh operation is initiated. Auto refresh, however, is not an operation performed at low power and is not discussed further. Power down, for example, is initiated when the die is idle (i.e., no open banks) and the clock enable signal CKE goes low.

[0028] FIG. 2 is a block diagram of a lower power control circuit 200, used in the SDRAM 100 (FIG. 1), constructed in accordance with an exemplary embodiment of the invention. The circuit 200 includes differential buffer enable logic 202, a differential buffer 204, four CMOS inverters 206, 208, 210, 214, a NAND gate 212 and self-refresh control circuitry 220.

[0029] The differential buffer enable logic 202 inputs a power down signal PWR_DWN and a self-refresh signal SELF_REFRESH. One, or both depending upon the chip specification, of these signals PWR_DWN, SELF_REFRESH are generated by the control logic 10 (FIG. 1) upon the occurrence of the appropriate commands. The differential buffer enable logic 202 also inputs an inverted clock enable signal CKE (TTL*) output from the first inverter 206 and a low power on signal LOW_POWER_ON from the self-

refresh control circuitry 220 (discussed below). The differential buffer enable logic 202 outputs an enable signal ENABLE to the differential amplifier 204. One value of the enable signal ENABLE enables the differential amplifier 204, a second value of the enable signal ENABLE disables the differential amplifier 204. In the illustrated embodiment, disabling the differential amplifier 204 causes the amplifier 204 to always have a logic high output.

[0030] The differential amplifier 204 is connected to receive the reference voltage Vref and the clock enable signal CKE. When enabled by the enable signal ENABLE, the differential amplifier 204 outputs the inverted value of the differential clock enable signal CKE relative to the reference voltage Vref (e.g., 0 if CKE ≥ Vref, 1 if CKE < Vref). This output signal is referred to as DA*. When disabled by the enable signal ENABLE, the differential amplifier 204 has a logic high output in this configuration. That is, DA* is high. When disabled, the differential amplifier 204 draws no current, which reduces power in the SDRAM. Furthermore, when the differential amplifier 204 is disabled, the reference voltage Vref may be floated or grounded since it is not being used. This reduces the power of the system even further.

[0031] When enabled by a self-refresh enabled signal SELF_REFRESH_ENABLED, the first inverter 206 inverts the clock enable signal CKE. This inverted clock enable signal is referred to as TTL* on FIG. 2. In the illustrated embodiment, when disabled by a self-refresh enabled signal SELF_REFRESH_ENABLED, the first inverter 206 always outputs a logic low TTL* signal. The output TTL* of the first inverter 206 is used as an input by

the third inverter 210. The output DA* of the differential amplifier 204 is used as an input by the second inverter 208. The outputs of the second and third inverter 208, 210 are used as inputs by the NAND gate 212. The output of the NAND gate 212 is used and inverted by the fourth inverter 214. The output of the fourth inverter 214 is a processed clock enable signal DDRSDRAM_CKE used by the self-refresh control circuitry 220. The processed clock enable signal DDRSDRAM_CKE will have the logic level of a properly generated clock enable signal CKE.

[0032] The self-refresh control circuitry 220 outputs the self-refresh enabled signal SELF_REFRESH_ENABLED and the low power on signal LOW_POWER_ON. The self-refresh control circuitry 220 also outputs signals to other circuitry on the DDR SDRAM that indicates that low power mode is being initiated (not shown).

[0033] The operation of the circuit 200 is now described with respect to FIGS. 3 and 5. In a normal mode of operation, the differential amplifier 204 is enabled (i.e., the enable signal ENABLE has a value that enables the amplifier 204), the reference voltage Vref is the specified reference voltage (i.e., not grounded or floated) and the first inverter 206 is disabled (i.e., the self-refresh enabled signal SELF_REFRESH_ENABLED has a value that disables the inverter 206). This means, that the first inverter 206 has a logic low TTL* signal. With this setup, the differential amplifier 204 is used to sense when the SDRAM should be placed into the low power mode (i.e., when the clock enable signal CKE is driven to a low logic level).

[0034] When the clock enable signal CKE is driven low by a low power command, the differential amplifier 204 detects the low level, inverts it and passes a high DA* signal (reference numeral 1 on FIG. 5) to the second inverter 208 (as discussed further, the signal is passed to the self-refresh control circuitry 220 and logic 202 which evaluates TTL* to see if it is tripped and disables the differential amplifier 204, if TTL* tripped). The second inverter 208 outputs a low logic level signal to its corresponding input of the NAND gate 212. The other input of the NAND gate 212 receives a high logic level signal, since the low level TTL* signal is inverted by inverter 210 and applied to the NAND gate 212. The NAND gate 212, having one low and one high input, outputs a high signal to the fourth inverter 214. The fourth inverter 214 outputs a low processed clock enable signal DDRSDRAM_CKE to the self-refresh control circuitry 220 (reference numeral 2 on FIG. 5).

[0035] The low processed clock enable signal DDRSDRAM_CKE is a signal to the self-refresh control circuitry 220 that self-refresh or power down is enabled (i.e., the clock enable signal CKE has been driven to a low logic level). The self-refresh control circuitry 220 outputs the self-refresh enabled signal SELF_REFRESH_ENABLED having a value that enables the first inverter 206. The self-refresh control circuitry 220 outputs the low power on signal LOW_POWER_ON to the differential buffer enable logic 202, which causes the differential buffer enable logic 202 to look at the state of TTL* (reference numeral 3 on FIG. 5). If TTL* is high (i.e., logic one), then the logic 202 outputs an enable signal ENABLE that disables the differential amplifier 204 (reference numerals 4 and 5 on FIG. 5). It should be noted that the

occurrence of the power down PWR_DWN or self-refresh SELF_REFRESH signals could also be used to generate an enable signal ENABLE that disables the differential amplifier 204 if so desired.

[0036] In low power mode, the clock enable signal CKE is low, which is eventually passed to the self-refresh circuitry 220 as a low processed clock enable signal DDRSDRAM_CKE. This signal causes the self-refresh control circuitry 220 to output the self-refresh enabled signal SELF_REFRESH_ENABLED having a value that enables the first inverter 206 (in this case keeps the inverter 206 enabled). The self-refresh control circuitry 220 outputs the low power on signal LOW_POWER_ON to the differential buffer enable logic 202 to ensure that the differential amplifier 204 remains disabled, which in the illustrated embodiment causes the differential amplifier 204 to output a high DA* signal to the input of the second inverter 208.

[0037] If a high clock enable signal CKE is received at the first inverter 206, indicating an attempt to switch out of the self-refresh or power down operations, the output TTL* of the first inverter 206 will go low (reference numerals 6, 8 on FIG. 5). The low signal is inverted by the third inverter 210 causing a high signal to be applied to its corresponding input of the NAND gate 212. Because the differential amplifier 204 applies a high DA* signal to the second inverter 208, the second inverter 208 outputs a low signal to the other input of the NAND gate 212. The NAND gate 212 continues to output a logic high signal causing the fourth inverter 214 to output a low processed clock enable signal DDRSDRAM_CKE. This keeps the DDRSDRAM circuitry

220 in the low power mode just in case there was noise or other glitches on the line carrying the clock enable signal. As such, the DDRSDRAM circuitry 220 continues to output the LOW_POWER_ON signal with a state indicating that low power is on and the SELF_REFRESH_ENABLED signal with a value that keeps the first inverter 206 enabled. This way, the SDRAM is kept in the low power mode just in case there was noise or other glitches on the line carrying the clock enable signal.

[0038] The low output TTL* of the first inverter 206 is also fed to the differential buffer enable logic 202, which causes the differential buffer enable logic 202 to output an enable signal ENABLE that enables the differential amplifier 204 (reference numerals 7, 9 on FIG. 5). At this point, both the differential amplifier 204 and the first inverter 206 are used to determine if the clock enable signal CKE has really been driven to the high logic level, which tells the SDRAM to exit the low power mode.

[0039] If a high clock enable signal CKE is no longer being generated, then the transition of the CKE signal was merely a glitch. As such, the TTL* will be high, causing the ENABLE signal to go low, which disables the differential amplifier 204 once again. This glitch is reflected in the timing diagram in the region indicated by arrow A. This region A shows that the low power control circuit 200 has glitch rejection up to the trip point of the differential amplifier 204 when a clock enable signal CKE spikes. The region in the timing diagram indicated by arrow B shows that the low power control circuit 200 has glitch rejection up to the trip point of the CMOS buffer 206 during low power mode (i.e., when Vref is grounded or floated).

[0040] If a high clock enable signal CKE is still being generated, it is received at the first inverter 206 and the differential amplifier 204. The first inverter 206 and the differential amplifier 204 output low signals (reference numerals 8, 10 on FIG. 5). The second and third inverters 208, 210 output high logic level signals to their respective inputs of the NAND gate 212. The NAND gate 212 outputs a logic low signal causing the fourth inverter 214 to output a high processed clock enable signal DDRSDRAM_CKE (reference numeral 11 on FIG. 5). As such, the DDRSDRAM circuitry 220 outputs the LOW_POWER_ON signal with a state indicating that low power is off and the SELF_REFRESH_ENABLED signal with a value that disables the first inverter 206 (reference numeral 12 on FIG. 5). This returns the SDRAM device to the normal power operating mode. The DDRSDRAM self-refresh circuitry 220 discontinues its self-refresh/power down operations.

[0041] The illustrated embodiment completely chokes off current to the differential amplifier 204 during the low power mode. To get out of the low power mode, the current must be reapplied to the amplifier, which must become operational and detect the clock enable signal CKE as described above within a certain specified period of time. Depending upon the timing requirements imposed by the industry standard, chip specification or application, a speedier response may be required. One exemplary solution, is to reduce the current flowing to the amplifier 204, instead of completely choking off the current, so that the amplifier 204 becomes operational much faster when the full current is reapplied. Thus, a tradeoff of slightly less power reduction versus increased operating speed is proposed.

[0042] FIG. 3 illustrates another lower power control circuit 300, used in the SDRAM 100 (FIG. 1), constructed in accordance with another exemplary embodiment of the invention. As is discussed below in more detail, the low power control circuit 300 can partially disable its differential amplifier 304 such that less power is consumed by the SDRAM, yet the amplifier 304 has a response time that is faster than completely choking off the amplifier 204 when enabled.

[0043] The low power control circuit 300 includes differential buffer enable logic 302, the differential amplifier 304, three CMOS inverters 306, 308, 310, a NAND gate 312, CMOS TTL receiver circuitry 350, and current producing circuits 360, 361, 371, 373.

[0044] The illustrated differential buffer enable logic 302 includes two NOR gates 332, 338, two inverters 336, 342, a NAND gate 340 and a switch 334. The first NOR gate 332 inputs a power down signal PWR_DWN and a self-refresh signal SELF_REFRESH. One, or both depending upon the chip specification, of these signals PWR_DWN, SELF_REFRESH are generated by the control logic 10 (FIG. 1) upon the occurrence of the appropriate commands. The output of the first NOR gate 332 is sent to inverter 336 and the second NOR gate 338. The output of inverter 336 is sent to NAND gate 340.

[0045] An ignore Vref signal IGNORE_VREF is also applied as an input to NAND gate 340. In a desired embodiment, the ignore Vref signal IGNORE_VREF is connected to an antifuse, or some other device such as a laser fuse or metal option, that is programmed based on the desired

application. The ignore Vref signal IGNORE_VREF will have one of two values and is discussed in more detail below. The second input of the second NOR gate 338 is connected to the TTL output from inverter 310 or a ground potential via the switch 334. That is, when the switch 334 is in a first position, the second NOR gate 338 inputs the TTL signal, but when the switch 334 is in the second position, the second NOR gate 338 inputs a logic low (from the ground potential). In a desired embodiment, the switch 334 (or fuse or metal option) is set during the manufacturing of the SDRAM (e.g., in a metal mask) based on the desired application for the SDRAM.

[0046] The values of the ignore Vref signal IGNORE_VREF and the position of the switch 334 will place the illustrated low power control circuit 300 into one of four operating modes as illustrated in Table I and discussed below in more detail below.

IGNORE_VREF	Switch 334	Operational Mode
GND	GND	Inverter 306 always disabled; Vref always a care; and amplifier 304 is "partially choked" (e.g., 25% reduction of current) in low power modes.
GND	TTL	Inverter 306 always disabled; Vref always a care; and amplifier 304's current is never reduced or choked off.
VCC	GND	Inverter 306 enabled in low power mode; Vref is a don't care while low power mode active; and amplifier 304 enters low power mode as "mostly choked" (e.g., %75% reduction of current).
VCC	TTL	Inverter 306 enabled in low power mode; Vref is a don't care while low power mode active; and amplifier 304 enters low power mode "mostly choked" (e.g., %75% reduction of current) only if CKE is low enough to trip inverter 306.

TABLE I

[0047] The output of NAND gate 340 is an enable TTL inverter signal EN_TTL*, which is applied to the CMOS TTL receiver circuitry 350. The output of the second NOR gate 338 is a low power LP signal, which is applied to the current producing circuits 360, 361, 371, 373. The low power signal LP is also applied to and inverted by inverter 342 to produce an inverted low power signal LP*, which is applied to the current producing circuits 360, 361, 371, 373.

[0048] The CMOS TTL receiver circuitry 350 includes two p-channel MOSFETs 344, 346 and two n-channel MOSFETs 348, 349. The first p-channel MOSFET 344 is connected between a supply voltage and the second p-channel MOSFET 346. The first p-channel MOSFET 344 has its gate coupled to the enable TTL inverter signal EN_TTL*. The second p-channel MOSFET 346 is connected to the first n-channel MOSFET 348 such that they form inverter 306.

[0049] The inverter 306 receives the clock enable signal CKE and inverts it to form the inverted clock enable signal TTL*. The enable TTL inverter signal EN_TTL* is also connected to the gate of the second n-channel transistor 349. The second n-channel transistor 349 is connected between the input of inverter 310 and ground. A logic high enable TTL inverter signal EN_TTL* causes the second n-channel transistor 349 to pull the input of inverter 310 to ground, causing the inverter 310 to output a high TTL signal. A logic low enable TTL inverter signal EN_TTL* causes the second n-channel transistor 349 to turn (or remain) off, allowing the inverted clock enable signal TTL* to be applied to the inverter 310 and the TTL signal to be applied to NAND gate 312.

[0050] One difference between the differential amplifier 304 of the illustrated embodiment and the amplifier 204 of the FIG. 2 embodiment is that the amplifier 304 of the illustrated embodiment is partially or mostly choked, if at all, rather than completely choked (as is done in the FIG. 2 embodiment). To do so, current producing circuits 360, 361, 371, 373 are used to supply high current, low current or very low current to the amplifier 304 and inverter 308.

[0051] The first current producing circuit 360 includes three n-channel MOSFETs 366, 368, 370. The first n-channel MOSFET 366 has its gate connected to the inverted low power signal LP*. When the inverted low power signal LP* has a value (i.e., high) that turns on the first n-channel MOSFET 366, a high current is applied to the differential amplifier 304. The second n-channel MOSFET 368 has its gate connected to the TTL signal from inverter 310. When the TTL signal has a value (i.e., high) that turns on the second n-channel MOSFET 368, a low current is applied to the differential amplifier 304. The third n-channel MOSFET 370 has its gate connected to the low power signal LP. When the low power signal LP has a value that turns on the third n-channel MOSFET 370, a very low current is applied to the differential amplifier 304.

[0052] The second current producing circuit 361 includes two p-channel MOSFETs 362, 364. The first p-channel MOSFET 362 has its gate connected to the low power signal LP. When the low power signal LP has a value (i.e., low) that turns on the first p-channel MOSFET 362, a high current is applied to the differential amplifier 304. The second p-channel MOSFET 364 has its gate connected to the inverted low power signal LP*. When the inverted low power signal LP* has a value (i.e., low) that turns on the second p-channel MOSFET 364, a very low current is applied to the differential amplifier 304.

[0053] It is the application of the currents from the current producing circuits 360, 361 that cause the amplifier to be: (1) fully enabled (i.e., high current); (2) disabled, yet powered by a low current (e.g., approximate %25

reduction of current); or (3) disabled, yet powered by a very low current (e.g., approximate %75 reduction of current).

[0054] The differential amplifier 304 inputs the clock enable signal CKE and the reference voltage Vref. The output of the differential amplifier 304 is fed to inverter 308. The output of inverter 308 is the differential clock enable signal DIFF. The output of the NAND gate 312 is a processed clock enable signal that is used by self-refresh control circuitry (such as the self-refresh control circuitry 220 of FIG. 2).

[0055] Inverter 308, comprised of two transistors 377, 378, is powered by the third and fourth current producing circuits 371, 373. The third current producing circuit 371 includes three p-channel MOSFETs 372, 374, 376. The first p-channel MOSFET 372 has its gate connected to the low power signal LP. When the low power signal LP has a value (i.e., low) that turns on the first p-channel MOSFET 372, a high current is applied to inverter 308. The second p-channel MOSFET 374 has its gate connected to ground and thus, a very low current is applied to the inverter 308 at all times. The third p-channel MOSFET 376 has its gate connected to the inverted TTL signal TTL* from inverter 306. When the inverted TTL signal TTL* has a value (i.e., low) that turns on the third p-channel MOSFET 376, a low current is applied to inverter 308.

[0056] The fourth current producing circuit 373 includes two n-channel MOSFETs 380, 382. The first n-channel MOSFET 380 has its gate connected to the inverted low power signal LP*. When the inverted low power signal LP* has a value (i.e., high) that turns on n-channel MOSFET 380, a high current is

applied to inverter 308. The second n-channel MOSFET 382 has its gate connected to the supply voltage and thus, a very low current is applied to inverter 308 at all times.

[0057] As set forth above in Table I, the operation of the illustrated low power control circuit 300 depends on the programming of the ignore Vref signal IGNORE_VREF and the position of the switch 334 in the differential enable logic 302. In one mode, low power mode is never entered (i.e., IGNORE_VREF is grounded and the switch 334 is connected to the TTL signal). In the other modes, low power mode is entered and the differential amplifier is either "partially choked" (i.e., approximately %25 reduction in applied current) or "mostly choked" (i.e., approximately %75 reduction in applied current). In the low power modes, the low power control circuit 300 operates essentially the same as the low power control circuit 200 illustrated in FIG. 2, with the exception of how the differential amplifier is disabled (i.e., partially or mostly choked in circuit 300 as opposed to completely choked in circuit 200). Otherwise, the logic is the same for entering the low power mode using the differential amplifier 304, using inverter 306 to detect an attempt to exit low power mode, using both inverter 306 and differential amplifier 304 to ensure that the clock enable signal CKE is driven to the value to exit low power mode, and exiting the low power mode (and disabling the inverter 306) in a specified amount of time.

[0058] FIG. 4 illustrates an exemplary processing system 900 which may utilize a memory device 100 constructed in accordance with an embodiment of the present invention. That is, the memory device 100 is a

DDR SDRAM or DDR SDRAM II device having a low power control circuit 200, 300 as illustrated in FIGS. 1-3.

[0059] The processing system 900 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0060] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one memory device 100 of the present invention. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory

controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0061] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, an miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and an legacy device interface 920. The primary bus bridge 903 may also coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0062] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers 919. The

legacy device interface 920 is used to couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0063] The processing system 900 illustrated in FIG. 4 is only an exemplary processing system with which the invention may be used. While FIG. 4 illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 and/or memory devices 100. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0064] The processes and devices described above illustrate preferred methods and typical devices of many that could be used and produced. The above description and drawings illustrate embodiments, which achieve the objects, features, and advantages of the present invention. However, it is not intended that the present invention be strictly limited to the above-described and illustrated embodiments. Any modification, though presently

unforeseeable, of the present invention that comes within the spirit and scope of the following claims should be considered part of the present invention.

[0065] What is claimed as new and desired to be protected by Letters Patent of the United States is: